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(54) Low power, ttl level CMOS input buffer with hysteresis.

(57) A circuit for use as a TTL level CMOS input buffer with hysteresis is disclosed. A first transistor (2) of a first conductivity type has its source connected to a first reference voltage. Second and third transistors (3,4) of opposite conductivity type have their source drain paths connected in series between the drain of the first transistor and a common potential. The gates of the first, second, and third transistors are connected to an input signal. An inverter (7) has its input connected to the drain of the first transistor and has an output. A fourth transistor (5) of the first conductivity type has its gate connected to the output, its drain connected to the series connection between the second and third transistors, and its source connected to a second reference voltage. By appropriately sizing the transistors, the low level trip point and the high level trip point of the circuit may be adjusted. The circuit draws lower power during standby. Logic gates may also be designed that incorporate the circuit.

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**LOW POWER, TTL LEVEL CMOS INPUT BUFFER WITH HYSTERESIS****FIELD OF THE INVENTION**

The invention is related to semiconductor integrated circuits and more particularly to input buffer circuits of the type used in CMOS semiconductor memory devices.

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**BACKGROUND OF THE INVENTION**

Dynamic random access memories (DRAMs) may be generally constructed as shown in U.S. Pat. No. 4,081,701 (a 16 kbit (DRAM) issued to White, McAdams and Redwine and assigned to Texas Instruments, Inc., and in U.S. Pat No. 4,239,993 (a 64 kbit DRAM) issued to McAlexander, White and Rao and assigned to Texas Instruments, Inc.

Complementary-metal-oxide (CMOS) semiconductor technology has been incorporated into the design of peripheral circuits for DRAMs. For example, U.S. Pat. No. 4,555,777 issued to Poteet and assigned to Texas Instruments, Inc. discloses DRAMs containing CMOS sense amplifiers. Among other advantages, CMOS technology aids in reducing the power consumed by the DRAM device.

An important consideration in the overall design of a memory system is the standby current drawn by a DRAM while it is inactive, since to a large degree this parameter determines the power consumed by the memory system. A significant portion of the standby current drawn by the DRAM comes from its first inverter connected to the Row Address Strobe (RAS) input. This inverter is required to be active (ie, powered up) at all times in order to respond to a RAS signal that initiates a cycle and when the system wants to refresh the dynamically stored data. However, with a voltage supply typically of 5v and transistor-transistor-logic (TTL) input signal levels (where typically 0.8v is a "low" signal and 2.4v is a "high" signal), CMOS input buffers consume current while in standby because the TTL "high" level input is not sufficient to turn the top p-channel transistor of its first CMOS inverter completely off. This allows a DRAM to consume power while in standby through a DC current path existing through the source/drain paths of the p-channel and n-channel transistors of the CMOS inverter of the input buffer.

Another important consideration in system design is the current consumed by a DRAM during initial power up before stable input voltage levels can be guaranteed. This problem occurs when the RAS input is at a level between the specified logic "low" and the specified logic "high". Between these levels, the input buffer may oscillate due to the RAS input fluctuating above and below the trip point of the first inverter of the input buffer. The trip point of the inverter is the level of voltage between the specified logic "low" and the specified logic "high" at which its p-channel transistor and its n-channel transistor switch. As RAS varies above and below this voltage level, the inverter accordingly varies as its transistors repeatedly switch on and off. This can cause the DRAM to go into oscillation that causes a large current drain on the external power supply. When this current drain is multiplied by the typically large number of memory chips located in a memory system, oscillation can load the system power supply and prevent it from coming up to the required voltage level in time.

It is an object of this invention to provide an input buffer that reduces the standby current drawn by a DRAM.

40 It is a further object of this invention to provide an input buffer that reduces DRAM oscillation.  
Other objects and benefits of this invention will be apparent to those skilled in the art, based upon the description to follow herein.

**SUMMARY OF THE INVENTION**

45 A circuit for use as a TTL level CMOS input buffer with hysteresis is disclosed. A first transistor of a first conductivity type has its source connected to a first reference voltage. Second and third transistors of opposite conductivity type have their source/drain paths connected in series between the drain of the first transistor and a common potential. The gates of the first, second, and third transistors are connected to an input signal. An inverter has its input connected to the drain of the first transistor and has an output. A fourth transistor of the first conductivity type has its gate connected to the output, its drain connected to the series connection between the second and third transistors, and its source connected to a second reference voltage. By appropriately sizing the transistors, the low level trip point and the high level trip point of the circuit may be adjusted. The circuit draws low power during standby. Logic gates may also be designed that incorporate the circuit.

## BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as other features and advantages thereof, will be best understood by reference to the detailed description that follows, wherein:

- 5 FIG. 1 is an electrical schematic diagram of the CMOS input circuit according to the invention.
- FIG. 2 is a graph illustrating hysteresis in the low level trip point and the high level trip point of the CMOS input circuit according to the invention.
- 10 FIG. 3 is a timing diagram for the circuit of FIG. 1 showing signal voltages at various nodes as a function of time with Vdd at 4.0v.
- FIG. 4 is a timing diagram for the circuit of FIG. 1 showing power consumption as a function of time with Vdd at 6.0v.
- 15 FIG. 5 is a timing diagram for the circuit of FIG. 1 showing slow ramp input signal transient analysis with temperature at 100C.
- FIG. 6 is a timing diagram for the circuit of FIG. 1 showing slow ramp input signal transient analysis with temperature at 0C.
- 20 FIG. 7 is an electrical schematic diagram of an alternative embodiment of the invention illustrating a single supply source for biasing node 10.
- FIG. 8 is an electrical schematic diagram of an alternative embodiment of the invention illustrating the addition of a pull-up transistor 8 to the embodiment of FIG. 7.
- 25 FIG. 9 is an electrical schematic diagram of an alternative embodiment of the invention illustrating the addition of an additional reference voltage to bias node 20 and the p-channel transistor of inverter 7.
- FIG. 10 is an electrical schematic diagram of an alternative embodiment of the invention illustrating its incorporation into a dual input clocked NOR logic gate.
- 30 FIG. 11 is an electrical schematic diagram of an alternative embodiment of the invention illustrating its incorporation into a dual input clocked NOR logic gate.
- FIG. 12 is an electrical schematic diagram of an alternative embodiment of the invention illustrating its incorporation into a dual input clocked NAND logic gate.
- FIG. 13 is an electrical schematic diagram of an alternative embodiment of the invention illustrating its incorporation into a dual input clocked NAND logic gate.

Corresponding numerals refer to corresponding parts in the figures unless the context otherwise indicates.

## DETAILED DESCRIPTION OF SPECIFIC EMBODIMENT

35 Referring to FIG. 1, a low power, TTL level CMOS input buffer with hysteresis according to the invention is disclosed that receives an input signal Vin and is responsive to yield an output signal Vout.

In FIG. 1, a CMOS inverter 6 is formed of a p-channel transistor 2 and an n-channel transistor 3 having their gates connected together at a node 50 and their drains connected together at a node 20. An n-channel 40 pull-up transistor 1 has its drain connected to a voltage supply Vdd, its gate connected to a voltage source Vref and its source connected to the source of p-channel transistor 2 at a node 10. The substrate of p-channel transistor 2 is also connected to node 10. Voltage supply Vdd is typically positive voltage such as +5v supplied by an external voltage supply source. However, Vdd may vary as is later explained. Voltage supply Vref is a stable steady voltage source. It may be produced by any manner that yields a stable 45 steady voltage. One way to produce Vref, for instance, is by means of a bandgap reference generator located on the DRAM chip. For the operation of the circuit of FIG.1 described herein, Vref has a value of positive 3.3v, however, the circuit of FIG. 1 advantageously accommodates other values for Vref as is later explained.

In the circuit of FIG. 1, also connected to node 50 is an input signal Vin and the gate of an n-channel 50 pull down transistor 4. Input signal Vin functions as the input signal to the circuit shown in FIG.1 and may be, for example, the Row Address Strobe (RAS) signal. The source of n-channel pull down transistor 4 is connected to ground and its drain is connected to the source of n-channel transistor 3 of CMOS inverter 6 at a node 30.

In FIG. 1, an inverter 7 with its input connected to node 20 yields the output signal Vout at node 40. 55 Connected to node 40 is the gate of a p-channel transistor 5. P-channel transistor 5 has both its source and its substrate connected to node 10 and provides feedback from node 40 to node 30 where its drain is connected.

The required range of Vref to insure that the circuit of FIG. 1 operates properly as a low power input

buffer within TTL levels (wherein typically 0.8v is a logic "low" signal and 2.4v is a logic "high" signal) during standby is found from the following relationships:

- (1)  $V_{ref} - V_{tn}(1) > \text{switching point of inverter } 7$
- (2)  $V_{ref} - V_{tn}(1) - V_{inh} < V_{tp}(2)$

5 where  $V_{tn}(1)$  denotes the threshold voltage of n-channel pull-up transistor 1,  $V_{tp}(2)$  denotes the absolute value of the threshold voltage of p-channel transistor 2 of CMOS inverter 6, and  $V_{inh}$  denotes the minimum "high" level of  $V_{in}$ . In modern CMOS integrated circuits, such as in high density DRAMs, a typical  $V_{tn}(1)$  is about 1.0v and a typical  $V_{tp}(2)$  is about 0.8-1.2v.  $V_{ref}$  may range between about 3.0v and 3.8v while satisfying the constraints of (1) and (2) above for  $V_{inh}$  as low as 2.0v.

10  $V_{dd}$ , as supplied by an external power supply source, often varies to some degree. For example, the specifications of modern DRAMs allow for plus or minus 10% margin on  $V_{dd}$ . In addition, the operation of the DRAM also generates noise on  $V_{dd}$ . The circuit of FIG. 1 advantageously yields output signal  $V_{out}$  within acceptable TTL range as  $V_{dd}$  varies from about 4.0v to 6.0v. As  $V_{dd}$  varies, n-channel pull-up transistor 1, connected as a source follower, causes the voltage at node 10 to remain essentially constant at 15  $V_{ref} - V_{tn}(1)$ . Stability of the input switching levels, relative to a wide variation in  $V_{dd}$ , advantageously occurs from the connection of the sources and substrates of p-channel transistors 2 and 5 to node 10 that maintains a stable level.

20 Through the addition of n-channel pull down transistor 4 and p-channel transistor 5, oscillation is advantageously controlled in FIG. 1 through the addition of hysteresis. The addition of hysteresis advantageously allows the input circuit of FIG. 1 to react to an expanded TTL input signal range, while yielding an acceptable TTL output signal.

25 FIG. 2 is a graph of input signal  $V_{in}$  and output signal  $V_{out}$  illustrating the addition of hysteresis in the input of FIG. 1. Solid line a illustrates a typical CMOS inverter with a single trip point,  $V_{trip}$ .  $V_{trip}$  is the switching point where a typical CMOS inverter switches as  $V_{in}$  goes high to low or low to high. Oscillation occurs in the typical CMOS inverter because  $V_{in}$  is typically not stable as  $V_{dd}$  fluctuates. As  $V_{in}$  varies slightly above and below  $V_{trip}$ , the typical CMOS inverter constantly switches in response thereto thus causing oscillation. In dashed line b, the high to low level switch point of the input of FIG. 1 is moved to the left of  $V_{trip}$ . The circuit now switches at  $V_{htrip}$  during the high to low transition of  $V_{in}$  rather than at  $V_{trip}$ . The dashed line c, the low to high level switch point of the input of FIG. 1 is moved to the right of  $V_{trip}$ . The 30 circuit now switches at  $V_{ltrip}$  during the low to high transition of  $V_{in}$  rather than at  $V_{trip}$ . Hysteresis results by separating  $V_{htrip}$  and  $V_{ltrip}$ . The circuit of FIG. 1 has 2 switching points, a low level switching point and a high level switching point. The addition of hysteresis moves the low level switching point closer to the TTL "low" level of 0.8v. The addition of hysteresis moves the high level switching point closer to the TTL "high" of 2.4v. Oscillation is reduced because variations of  $V_{in}$  are handled so that larger variations are 35 needed to cause switching.

The low level trip point and the high level trip point of inverter 6 of FIG. 1 is governed by the relative sizing of the widths and lengths of transistors 2, 3, 4, and 5. By appropriately sizing the widths and lengths, these transistors are advantageously set to switch on and off at different voltage levels. The low level trip point of inverter 6 is controlled by the relative sizing of p-channel transistor 2 and n-channel transistors 3 40 and 4. The high level trip point of inverter 6 is controlled by the relative sizing of n-channel pull-down transistor 4 and p-channel transistor 5. To a smaller degree, the relative sizing of p-channel transistor 2 and n-channel 3 of inverter 6 also play a role in controlling the high level trip point.

45 The operation of the input circuit shown in FIG. 1 has been simulated and will now be described in detail. Referring to FIG. 3, a timing diagram of the circuit of FIG. 1 is illustrated with the temperature equaling 100C,  $V_{dd}$  equaling 4.0v,  $V_{ref}$  equaling 3.3v, input signal  $V_{in}$  varying from 1.2v to 2.1v and the circuit elements of FIG. 1 having the following values:

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n-channel pull-up transistor 1 ----width = 30 microns;
---length = 0.8 microns;
5 p-channel transistor 2 -----width = 05 microns;
---length = 0.8 microns;
n-channel transistor 3 -----width = 05 microns;
---length = 01.2 microns;
10 n-channel pull-down transistor 4----width = 05 microns;
---length = 01.2 microns;
p-channel transistor 5 -----width = 12 microns;
15 ---length = 01.2 microns;
inverter 7 (p-channel transistor)---width = 10 microns;
---length = 0.8 microns;
20 (n-channel transistor)---width = 30 microns;
---length = 0.8 microns.

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With the above width to length ratios, it is seen that n-channel transistors 3 and 4 are smaller than p-channel transistors 2 and 5. The low level trip point of inverter 6 is about 1.2v and the high level trip point of inverter 6 is about 2.0v. Input Signal Vin and output signal Vout, and Vn20 (the voltage at node 20) are illustrated in FIG. 3. Previous to time t0, input signal Vin is "high", at 2.1v. P-channel transistor 2 is off and n-channel transistor 3 is on. N-channel pull-down transistor 4 is also on. Vn20 is pulled "low" through the source/drain paths of n-channel transistor 3 and n-channel pull-down transistor 4. Vn20 is complemented by inverter 7 to yield a "high" output signal Vout at node 40 of 4.0v. N-channel pull-up transistor 1 remains on at all times, pulling the voltage at node 10 high to a level of Vref - Vtn(1). P-channel transistor 5 has output signal Vout "high" applied at its gate and is therefore off.

In FIG. 3, at time t0, a "high" to "low" transition occurs. Input signal Vin drops "low" to a level of 1.2v. The impedance of N-channel transistor 4 rises and allows P-channel transistor 2 to control node 20. P-channel transistor 2 of inverter 6 turns on, the absolute value of the voltage level on its gate now greater than the threshold voltage of P-channel transistor 2. The voltage at node 20 rapidly rises towards the voltage at node 10. Inverter 7 complements the voltage at node 20 as it rises so output signal Vout goes "low". P-channel transistor 5 provides feedback from node 40 to node 30. As output signal Vout goes "low", once the gate to source voltage of p-channel transistor 5 rises above its threshold voltage, p-channel transistor 5 turns on and allows node 30 to rise towards the voltage at node 10. As node 30 rises, transistor 3 will turn off as input signal Vin drops below Vn20. (For n-channel transistor 3 to be on, its gate voltage must be a threshold voltage above its source voltage.)

In FIG. 3, at time t1, a "low" to "high" transition occurs. Input signal Vin goes "high" to a level of 2.1v. P-channel transistor 2 turns off, n-channel pull down transistor 4 turns on and pulls the voltage at node 30 down. Once the voltage at node 30 becomes a threshold voltage less than input signal Vin, n-channel transistor 3 begins to pull the voltage at node 20 down. The voltage at node 20 is complemented by inverter 7. As output signal Vout rises, transistor 5 turns off and n-channel pull down transistor 4 is better able to pull the voltages at nodes 30 and 20 low.

FIG. 4 is a timing diagram of the input circuit of Fig. 1 illustrating the low power it consumes. Vdd is now increased to 6.0v in this simulation. All other parameters have the same values as those in the example of FIG. 3 above explained. Voltage is shown on the solid vertical axis. Amperage is shown on the segmented vertical axis. By comparing FIG. 4 with FIG. 3, as explained above, Vn20 rises to the same level as in FIG. 3 although Vdd is substantially increased. Vout now rises to a "high" level signal of 6.0v. When Vout is "high", Idd is essentially 0mA. When Vout is "low", Idd is approximately -0.6mA. The power drawn by the circuit during standby is very low.

FIG. 5 is a timing diagram for the input circuit of FIG. 1 showing scan range input signal transient analysis. In this simulation, input signal Vin slowly ramps upward from 0v at t0 to 4v at t2. At t1, with Vin having a value of about 2.1v, the circuit recognizes input signal Vin as being "high". The "high" level trip

point of inverter 6 is reached, n-channel transistors 3 and 4 are on and Vn20 drops to 0v. Output signal Vout rises to 4.0v with Vdd of 4.0 v, or to 6.0 v, with Vdd of 6.0v. At t2, input signal Vin begins to decline. Output signal Vout remains "high" until input signal Vin drops to the "low" level trip point of inverter 6 of about 1.2v. P-channel transistor 6 turns on, n-channel transistors 3 and 4 turn off, and Vn20 rises. Output signal Vout drops low to 0v.

FIG. 6 is a timing diagram for the input circuit of FIG. 1 showing scan range input signal transient analysis with a temperature of 0C. By comparing FIG. 6 with FIG. 5, it is seen that the hysteresis in this simulation increases when the circuit operates at the lower temperature. The "high" level switch point of inverter 6 is at about 1.8v rather than 2.0v.

FIG. 7 is an electrical schematic diagram illustrating an alternative embodiment of the invention wherein FIG. 1 is modified so that Vdd now supplies the gate of n-channel pull up transistor 1 in place of Vref. This circuit embodiment is advantageous for situations wherein a stable reference voltage is not available. This circuit operates as above described except that the voltage at node 10 is not as steady and will now vary as Vdd fluctuates.

FIG. 8 is an electrical schematic diagram illustrating an alternative embodiment of the invention wherein FIG. 7 is modified by the addition of a p-channel pull-up transistor 8. P-channel pull-up transistor 8 has its gate connected to node 40 and its source/drain path connected between node 20 and Vdd. In this embodiment, p-channel pull-up transistor 8 is a narrow width/long channel (small) transistor so that its impedance is large when it is on. (P-channel pull-up transistor 8 is on when output signal Vout drops "low" corresponding to input signal Vin dropping "low".) P-channel pull-up transistor 8 provides feedback from node 40 to node 20 that helps turn the p-channel transistor, not shown, of inverter 7 off by pulling the node 20 to Vdd. This helps bring Idd of FIG. 4 closer to zero between times t0 and t1 when input signal Vin is "low".

FIG. 9 is an electrical schematic diagram illustrating an alternative embodiment of the invention wherein FIG. 1 is modified by the addition of a p-channel pull-up transistor 8 and a second reference voltage Vref2. In this embodiment, the source and substrate of p-channel transistor 5 and the substrate of p-channel transistor 2 are not connected to node 10, rather, they are connected to Vref2. Vref2 is a stable reference voltage source. It may be generated, for instance, by a bandgap generator circuit located on the DRAM chip. Vref2 in this example has a value of 4.0v. Vref1 has a value of 3.3v as earlier described. P-channel pull-up transistor 8 has its gate connected to node 40 and its source/drain path connected between Vref2 and node 20. The substrate of p-channel transistor 8 is also connected to Vref2. This embodiment will also function in the case wherein Vref2 is lower than Vref1.

The embodiment illustrated in FIG. 9 is advantageous in situations where stable reference voltage sources are available. As illustrated in FIG. 4, between time t0 and t1, when input signal Vin is low, the circuit of FIG. 1 draws a small amount of Idd. This occurs because the voltage at node 20 is not quite large enough to completely turn off the p-channel transistor, not shown, of inverter 7. Vref2 supplies enough voltage to turn the p-channel transistor, not shown, of inverter 7 off during the time when input signal Vin is low. This brings Idd closer to zero and further reduces the power drawn by the circuit.

The invention may be used in the design of logic gates. FIG. 10 is an electrical schematic of a dual input clocked NOR gate. The embodiment disclosed in FIG. 1 is modified as follows: The source of p-channel transistor 5 is disconnected from node 10 and is connected to Vdd. A p-channel pull-up transistor 8 is added having its gate connected to node 40 and its source/drain path connected between Vdd and node 20. P-channel transistors 9a and 9c, connected in series, are added having their source/drain paths connected between Vdd and the drain of n-channel transistor 1. N-channel transistors 9b and 9d, are connected between Vdd and ground. Input signal CMOS1 is connected to the gate of p-channel transistor 9c and n-channel transistor 9d. Input signal CMOS2 is connected to the gate of p-channel transistor 9a and n-channel transistor 9b. The circuit operates as a NOR logic gate that is clocked by input signal Vin. Output signal Vout is responsive to input signal Vin when both input signals CMOS1 and CMOS2 are low.

FIG. 11 is an electrical schematic diagram of a dual input clocked NOR gate also. Figure 10 is modified as follows: N-channel pull-up transistor 1 now has its drain connected to Vdd and p-channel transistors 9a and 9c, connected in series, now have their source/drain paths connected between the source of n-channel pull-up transistor 1 and the series source/drain path of p-channel transistor 2 and n-channel transistor 3. This circuit also operates as a NOR logic gate that is clocked by input signal Vin.

FIG. 12 is an electrical schematic diagram of a dual input clocked NAND gate. The embodiment disclosed in FIG. 1 is modified as follows: The source of p-channel transistor 5 is disconnected from node 10 and is connected to Vdd. A p-channel pull-up transistor 8 is added having its gate connected to node 40 and its source/drain path connected between Vdd and node 20. P-channeltransistor 9a receives input signal

CMOS2 on its gate. P-channel transistor 9c receives input signal CMOS1 on its gate. P-channel transistors 9a and 9c are connected in parallel between Vdd and node 20. N-channel transistor 9d receives input signal CMOS1 on its gate. N-channel transistor 9b receives input signal CMOS2 on its gate. N-channel transistors 9d and 9b are connected in series between the source of n-channel transistor 4 and ground. The circuit 5 functions as a NAND gate. Output signal Vout is responsive to input signal Vin when input signals CMOS1 and CMOS2 are high.

FIG. 13 is also an electrical schematic diagram of a dual input clocked NAND gate. The embodiment disclosed in FIG. 1 is modified as follows: The source of p-channel transistor 5 is disconnected from node 10 and is connected to Vdd. A p-channel pull-up transistor 8 is added having its gate connected to node 40 10 and its source/drain path connected between Vdd and node 20. P-channel transistor 9a receives input signal CMOS2 on its gate. P-channel transistor 9c receives input signal CMOS1 on its gate. P-channel transistors 9a and 9c are connected in parallel between Vdd and node 20. N-channel transistor 9d receives input signal CMOS1 on its gate. N-channel transistor 9b receives input signal CMOS2 on its gate. N-channel transistors 9b and 9d are connected in series between the series connection of p-channel transistor 2 and n-channel 15 transistor 3. The circuit functions as a NAND gate. Output signal Vout is responsive to input signal Vin when input signals CMOS1 and CMOS2 are high.

While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various other embodiments of the invention will be apparent to persons skilled in the art upon reference to this description. It is therefore contemplated that the 20 appended claims will cover any such modification or embodiments as fall within the true scope of the invention.

### Claims

25 1. An input circuit comprising:

A first transistor of a first conductivity type having its source connected to a first reference voltage, its gate connected to an input signal, and having a drain;

30 second and third transistors of an opposite conductivity type having their source/drain paths connected in series between the drain of said first transistor and a common potential, and having their gates connected to the input signal;

an inverter having its input connected to the drain of said first transistor, and having an output; and

35 a fourth transistor of said first conductivity type having its gate connected to the output, its drain connected to the series connection between said second and third transistors, and having its source connected to a second reference voltage.

40 2. The circuit of claim 1 further comprising:

a first pull-up transistor of the opposite conductivity type having its drain connected to a voltage supply, its gate connected to a voltage reference generator circuit and its source connected to the source of the first transistor.

45 3. The circuit of claim 2 further comprising:

a second pull-up transistor of the first conductivity type having its source connected to the voltage supply, its drain connected to the input of the inverter, and its gate connected to the output.

50 4. The circuit of claim 3 further comprising:

logic circuitry having a logic input and coupled to the input of the inverter in such a manner that the inverter is also responsive to the state of the logic input of the logic circuitry.

55 5. The circuit of claim 4 wherein said logic circuitry comprises:

a first logic transistor of the first conductivity type having its gate connected to the logic input, and its

source/drain path connected in series between the voltage supply and the input of the inverter; and

a second logic transistor of the second conductivity type having its gate connected to the logic input, and its source/drain path connected in series between the drain of the first transistor and the common potential.

5       6. The circuit of claim 3 wherein said logic circuitry comprises:

10      a first logic transistor of the first conductivity type having its gate connected to the logic input, and its source/drain path connected in series between the voltage supply and the drain of the first pull-up transistor; and

15      a second logic transistor of the second conductivity type having its gate connected to the logic input, and its source/drain path connected in series between the input of the inverter and the common potential.

7. The circuit of claim 3 wherein said logic circuitry comprises:

20      a first logic transistor of the first conductivity type having its gate connected to the logic input, and its source/drain path connected in series between the source of the first pull-up transistor and the source of the first transistor; and

25      a second logic transistor of the second conductivity type having its gate connected to the logic input, and its source/drain path connected in series between the input of the inverter and the common potential.

8. An input circuit comprising:

30      a pull-up transistor having its source/drain path connected in series between a first reference voltage and an intermediate output node, and having its gate connected to an input signal, its source/drain path being conductive responsive to the input signal being at a first logic state;

35      a first and second pull-down transistors having their source/drain paths connected in series between the intermediate output node and a common potential, and having their gates connected to the input signal, their source/drain path being conductive responsive to the input signal being at a second logic state;

40      an inverter having its input connected to the intermediate output node, to produce an output signal; and

45      a feedback transistor having its gate connected to the output signal, and its source/drain path connected in series between a second reference voltage and the series connection between the first and second pull-down transistors, its source/drain path being conductive responsive to the logic state of the output signal.

45      9. The circuit according to claim 8 wherein the relative sizes of the pull-up transistor, and the first and second pull-down transistors cause the output signal to begin the change from the second logic state to a first logic state responsive to the input signal crossing a first voltage in changing from the second logic state to the first logic state.

50      10. The circuit according to claim 8 wherein the relative sizes of the second pull-down transistor and the feedback transistor cause the output signal to begin to change from a first logic state to a second logic state responsive to the input signal crossing a second voltage in changing from the first logic state to the second logic state.

55      11. The circuit according to claim 9 wherein the relative sizes of the second pull-down transistor and the feedback transistor cause the output signal to begin to change from a first logic state to a second logic state responsive to the input signal crossing a second voltage in changing from the first logic state to the second logic state.

12. The circuit of claim 8 further comprising:

a second pull-up transistor having its source/drain path connected in series between a voltage supply and source/drain path of the pull-up transistor , and having its gate connected to a voltage reference generator circuit, its source/drain path being always conductive.

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13. The circuit of claim 12 further comprising:

10 a third pull-up transistor having its source/drain path connected between the voltage supply and the input of the inverter, and having its gate connected to the output.

14. A CMOS input buffer comprising:

15 a pull-up transistor having its source/drain path connected in series between a voltage supply and a first reference voltage, and having its gate connected to a reference voltage generator circuit;

a CMOS inverter having the source/drain paths of its p-channel transistor and its n-channel transistor connected in series between the first reference voltage and a node, and having the gates of its p-channel transistor and its n-channel transistor connected to the input signal;

20 a pull-down transistor having its source/drain path connected in series between a common potential and the node;

25 an inverter having its input connected to the source/drain path of the CMOS inverter, and having an output;

a feedback transistor having its gate connected to the output, and its source/drain path connected in series between a second reference voltage and the node; and

30 15. The CMOS input buffer of claim 14 further comprising:

a second pull-up transistor having its source/drain path connected in series between the voltage supply and the input of the inverter and having its gate connected to the output.

35 16. The circuit of any preceding claim, wherein the first reference voltage and the second reference voltage are the same.

17. The circuit of any of claims 1-15, wherein the second reference voltage is higher than the first reference voltage.

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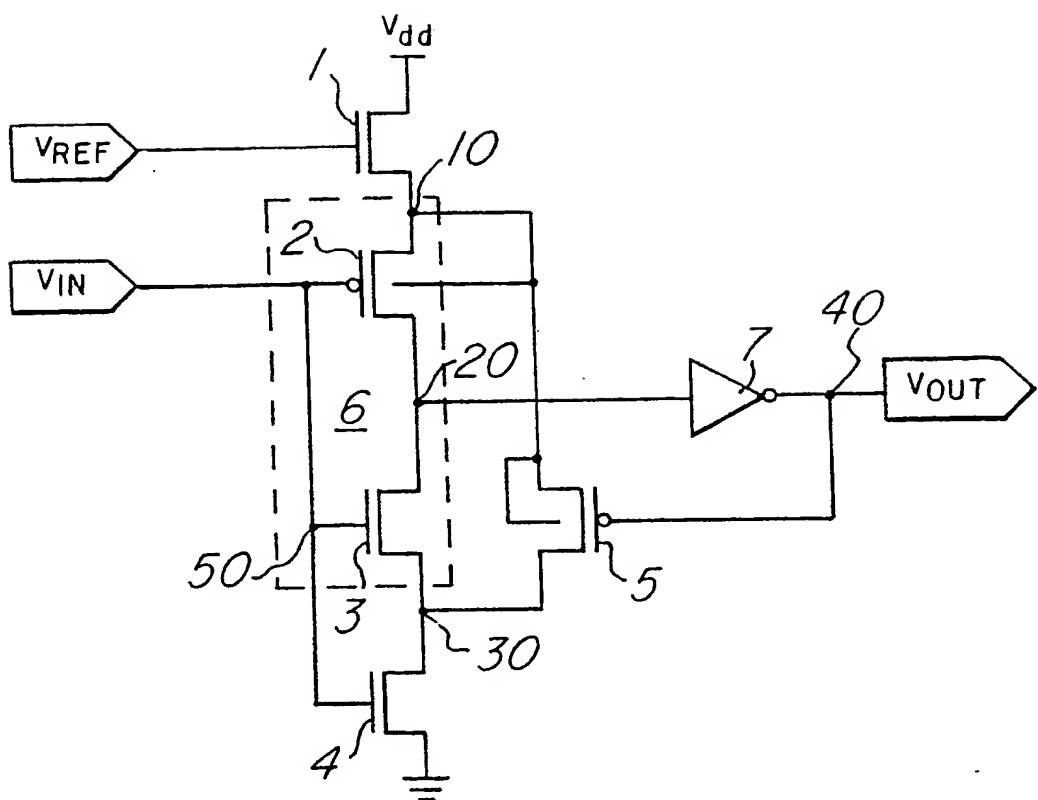


Fig. 1

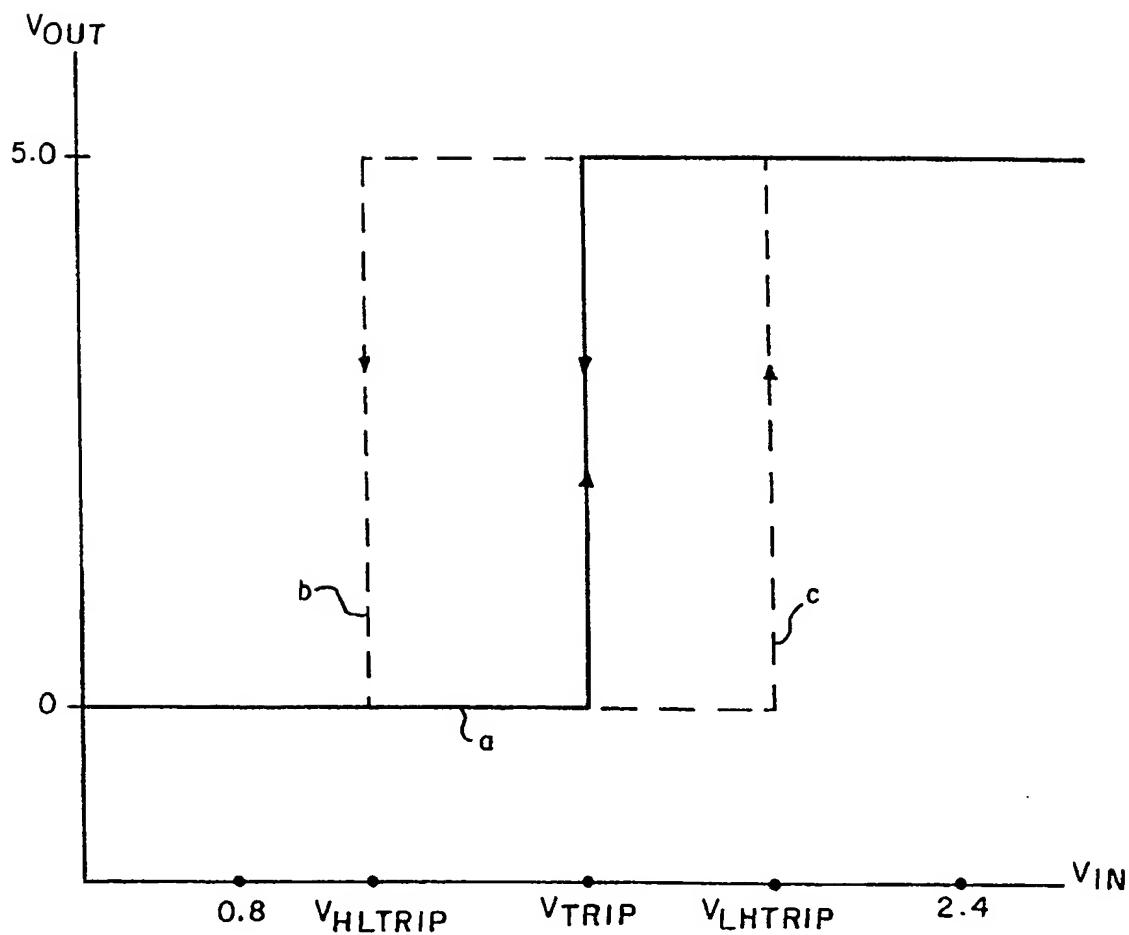


Fig.2

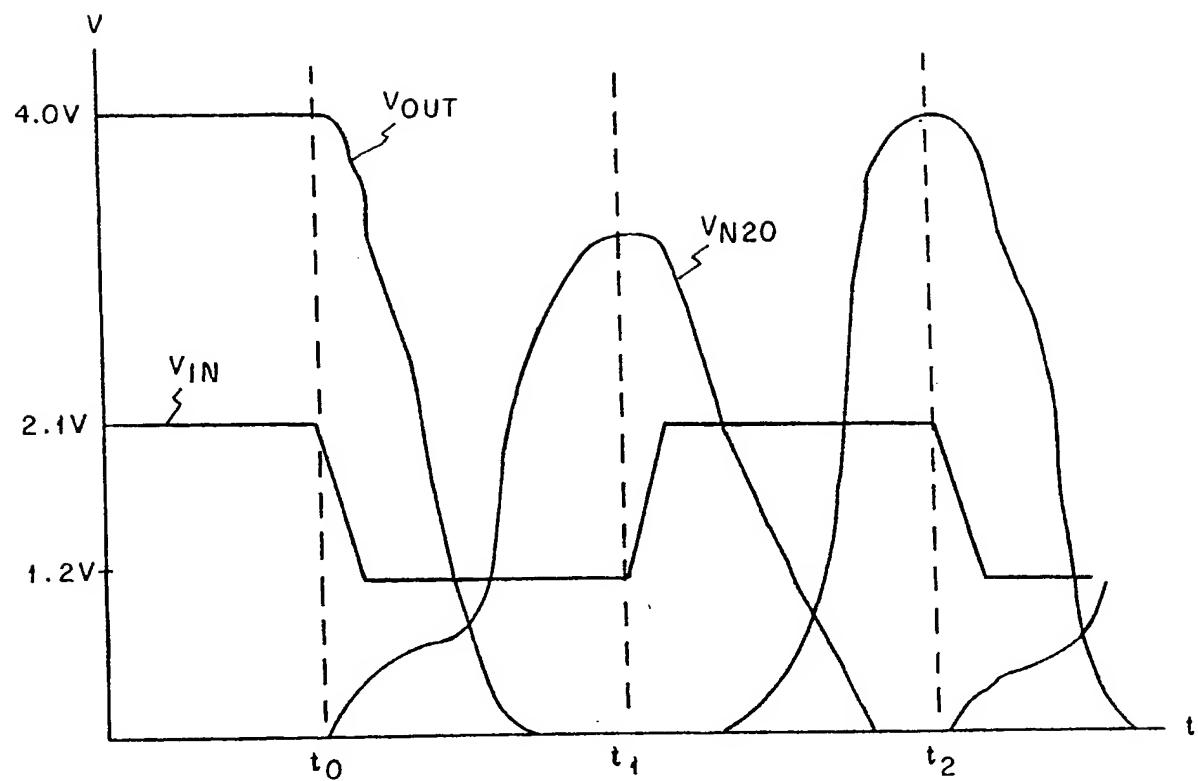


Fig.3

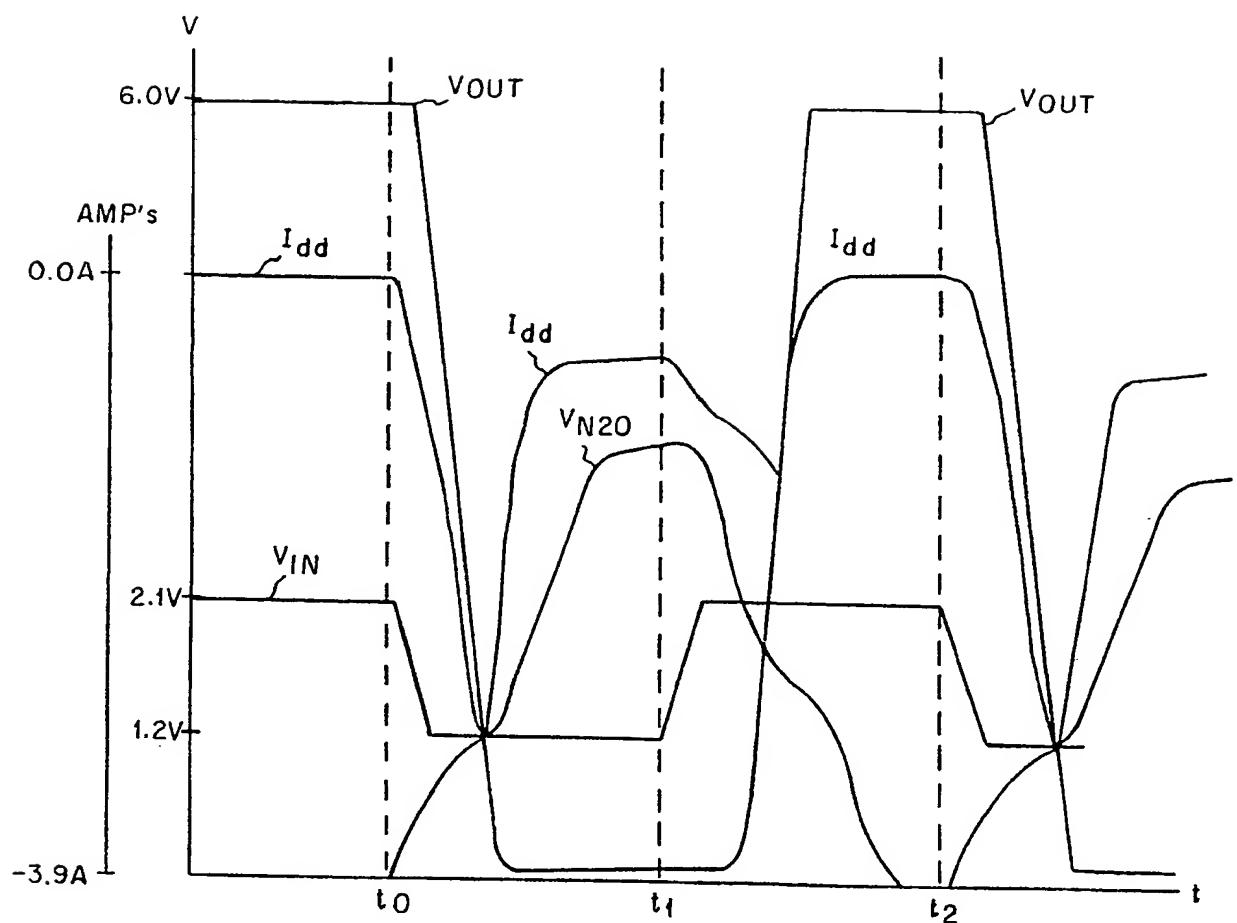


Fig.4

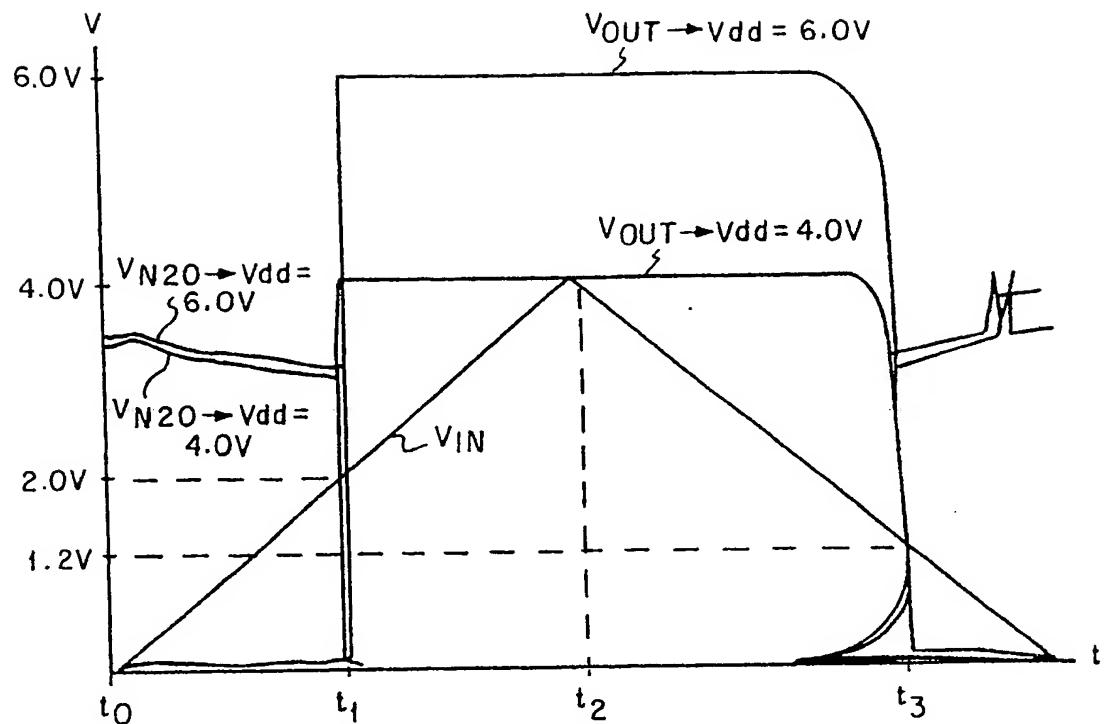


Fig. 5

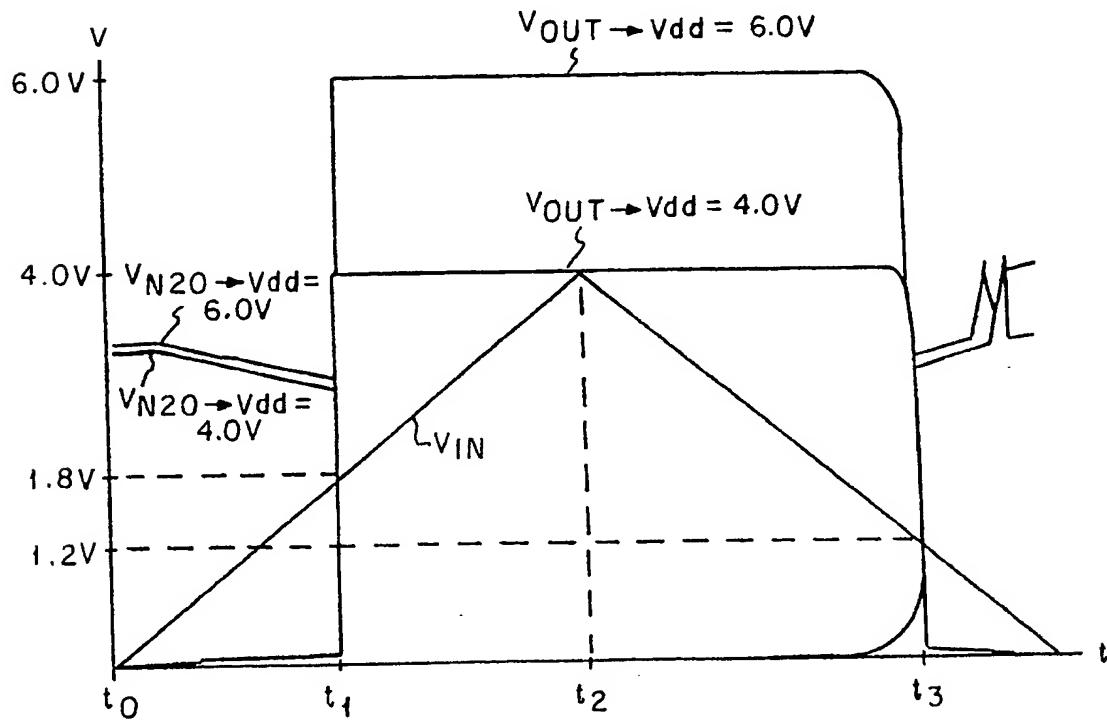


Fig. 6

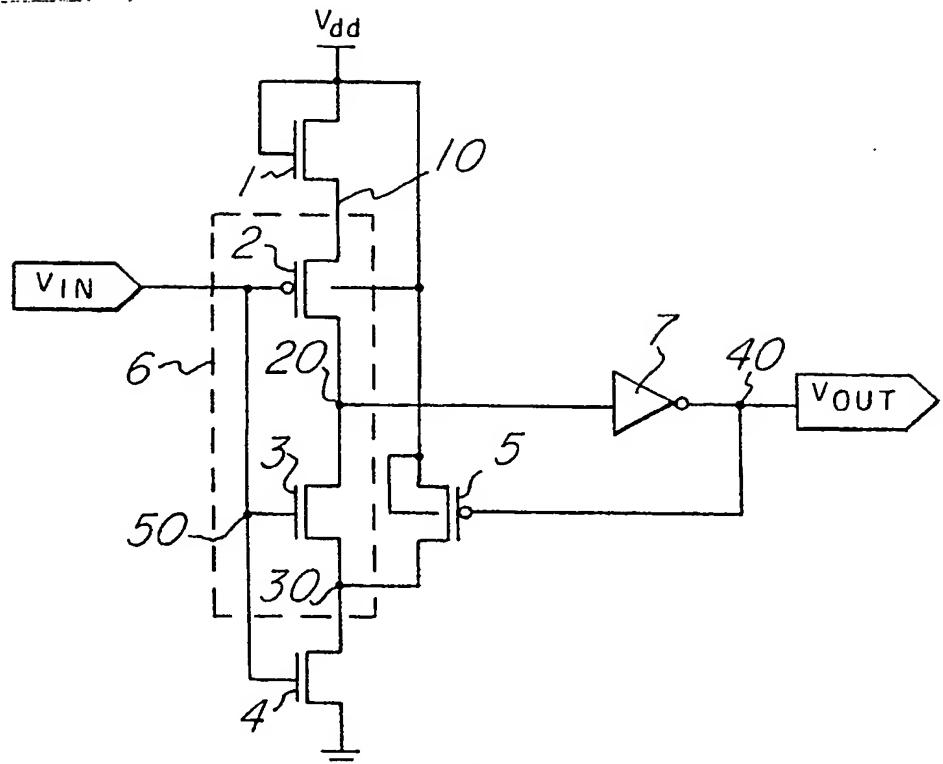


Fig.7

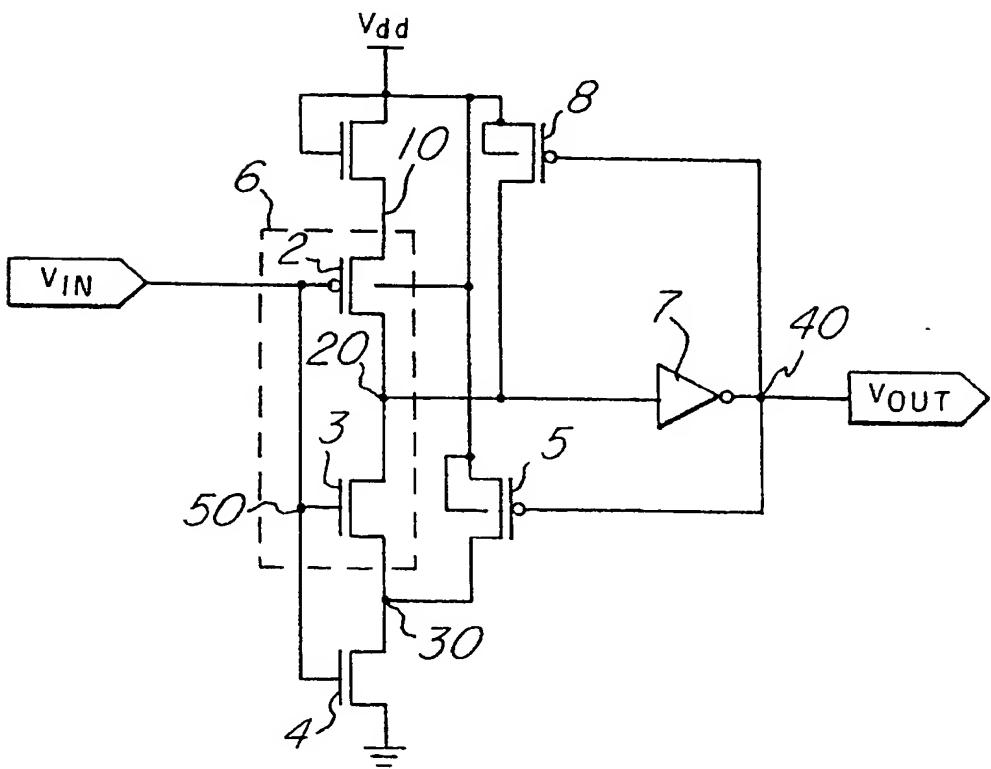


Fig.8

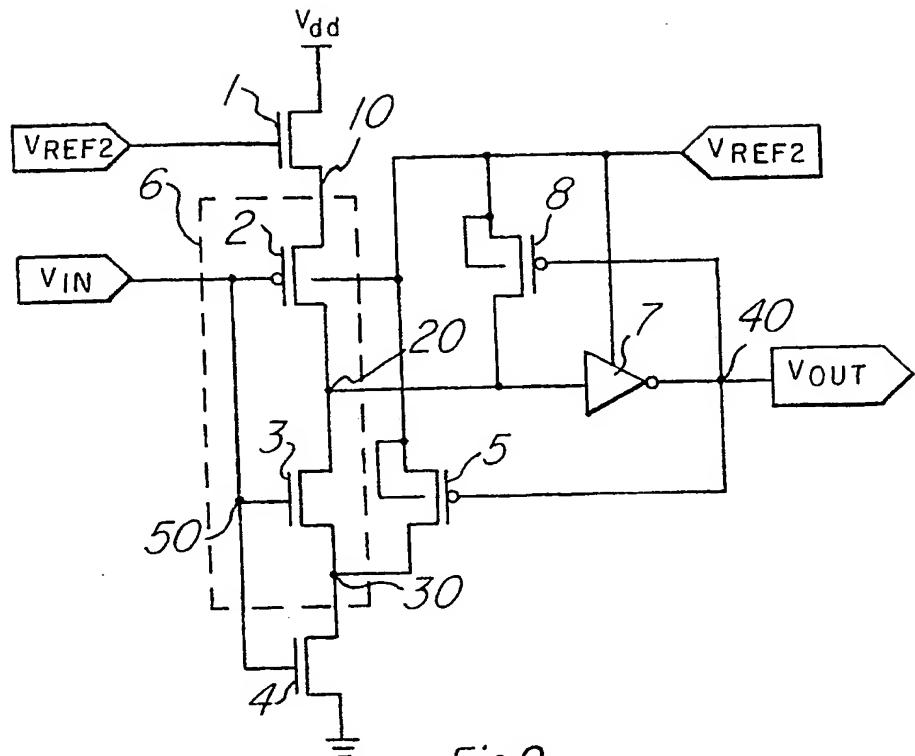


Fig.9

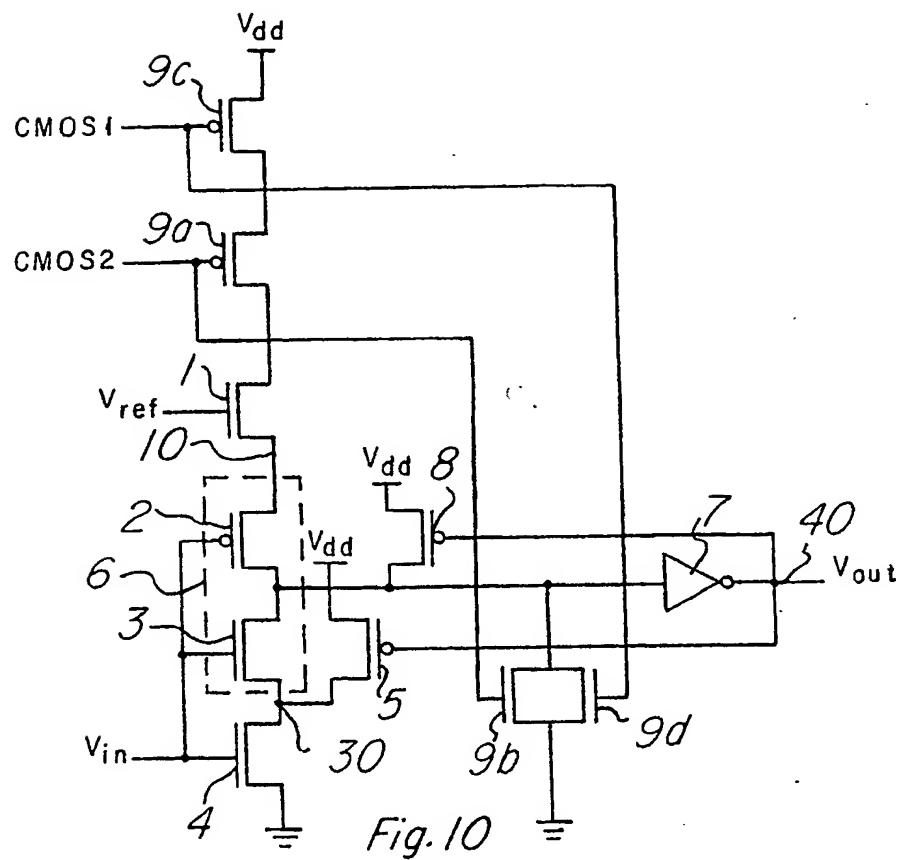


Fig.10

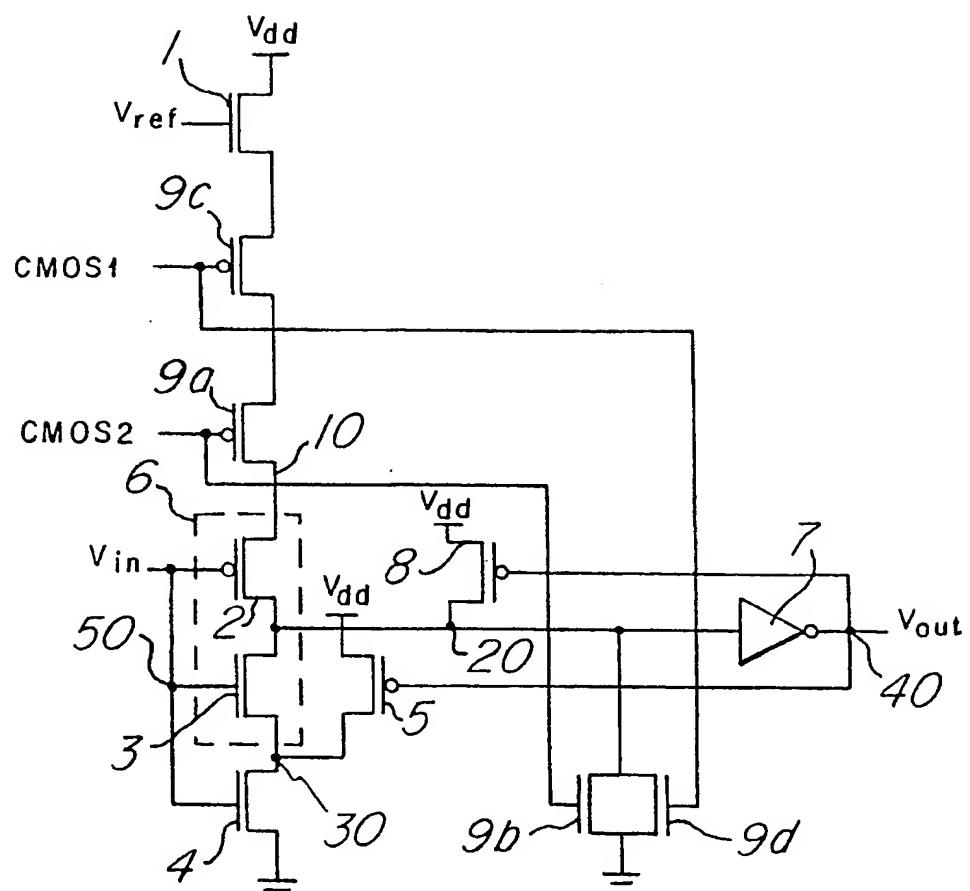


Fig. 11

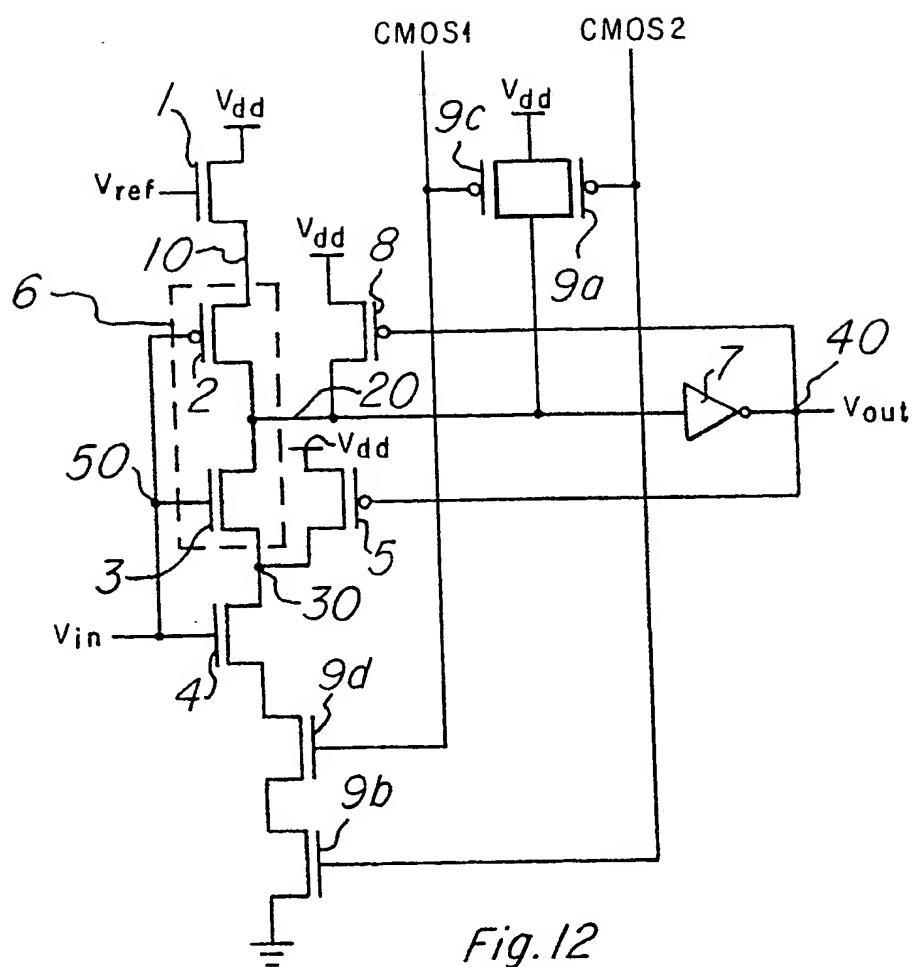


Fig. 12

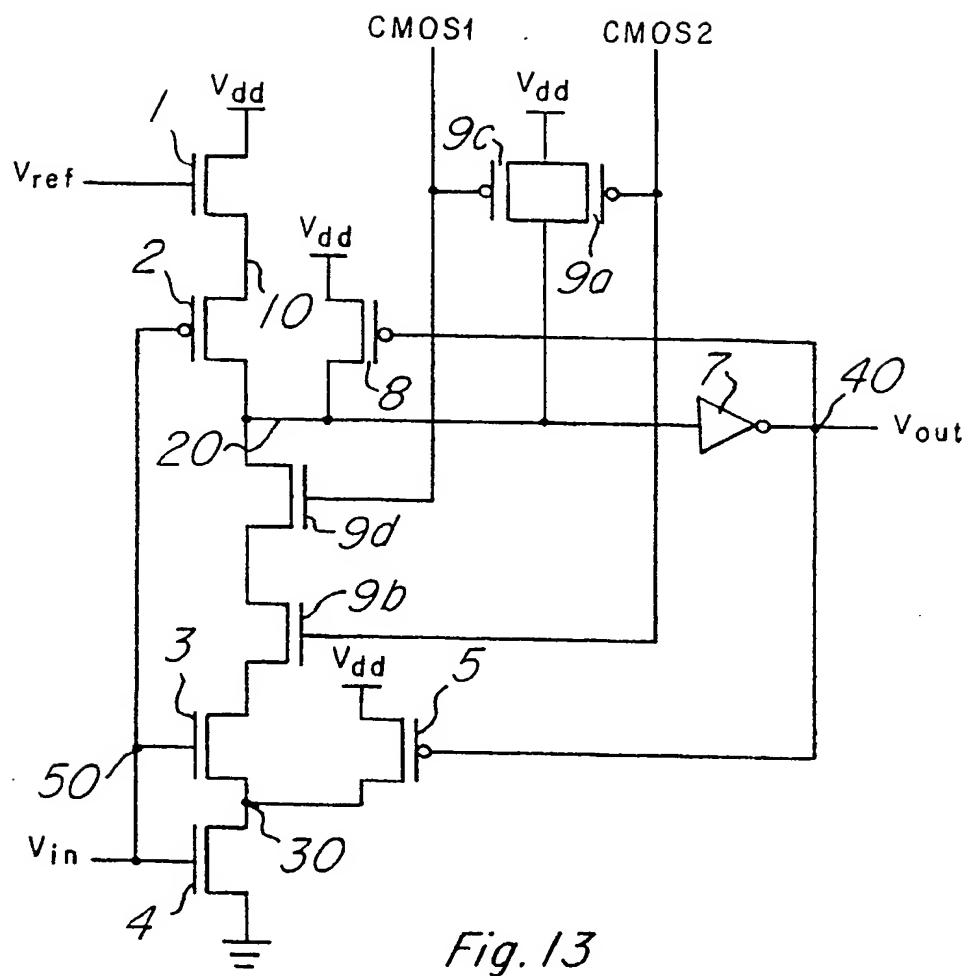


Fig. 13

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(54) Low power, ttl level CMOS input buffer with hysteresis.

(57) A circuit for use as a TTL level CMOS input buffer with hysteresis is disclosed. A first transistor (2) of a first conductivity type has its source connected to a first reference voltage. Second and third transistors (3,4) of opposite conductivity type have their source drain paths connected in series between the drain of the first transistor and a common potential. The gates of the first, second, and third transistors are connected to an input signal. An inverter (7) has its input connected to the drain of the first transistor and has an output. A fourth transistor (5) of the first conductivity type has its gate connected to the output, its drain connected to the series connection between the second and third transistors, and its source connected to a second reference voltage. By appropriately sizing the transistors, the low level trip point and the high level trip point of the circuit may be adjusted. The circuit draws lower power during standby. Logic gates may also be designed that incorporate the circuit.

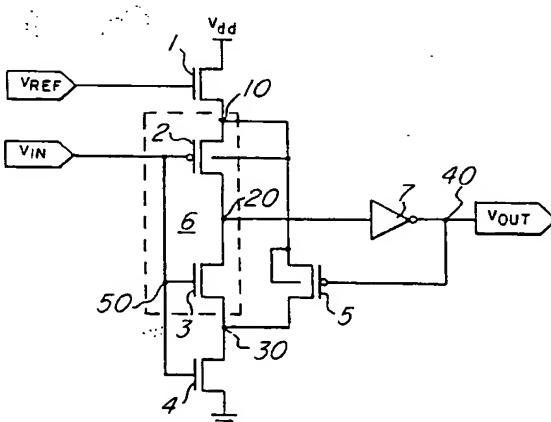


Fig. 1

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REPORT

Application Number

EP 90 31 3086

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)		
X	US-A-4 464 587 (SUZUKI ET AL.) * column 5, line 48 - column 8, line 16; figures 13,16,20 **	1,8-11, 14,16 2-7,12, 13,15	H 03 K 3/353		
Y	-----	2-7,12, 13,15			
Y	US-A-4 563 595 (BOSE) * column 2, line 17 - column 3, line 51; figure 1 ** -----				
The present search report has been drawn up for all claims			TECHNICAL FIELDS SEARCHED (Int. Cl.5)		
			H 03 K		
Place of search	Date of completion of search	Examiner			
The Hague	20 December 91	CANTARELLI R.J.H.			
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